Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1.A mixed-mode process for integration circuits comprising:
providing a semiconductor substrate, a surface of the semiconductor substrate comprising at least a first conductor formed in a first conductive region, at least a second conductor formed in a second conductive region, at least a metal-oxide-semiconductor (MOS) transistor formed in a MOS transistor region, and at least a capacitor formed in a capacitor region;
forming a mask on the semiconductor substrate to cover the MOS transistor, the first conductor, and the capacitor and to expose the second conductor;
performing a first etching process to remove a specific thickness of the second conductor; and
performing a first ion implantation process to dope the second conductor with first type dopants.

[c2] 2.The mixed-mode process of claim 1 further comprising the following steps for forming the first conductor, the second conductor, the MOS transistor, and the capacitor:
sequentially forming a gate oxide layer and a first

polysilicon layer on the semiconductor substrate;
performing a first photo-etching-process (PEP) to remove portions of the first polysilicon layer to simultaneously form a gate structure and a bottom electrode plate structure of the capacitor respectively in the MOS transistor region and the capacitor region;
sequentially forming an inter polysilicon oxide (IPO) layer and a second polysilicon layer doped with second type dopants on the semiconductor substrate to cover the gate structure and the bottom electrode plate structure;
performing a second PEP to remove portions of the second polysilicon layer to form the first conductor, the second conductor, and a top electrode plate of the capacitor, respectively, in the first conductive region, the second conductive region, and the capacitor region;
forming a dielectric layer on the semiconductor substrate to cover the first conductor, the second conductor, the gate structure, and the capacitor; and
performing a second etching process to remove portions of the dielectric layer to form a spacer on either sides of the first conductor, the second conductor, the capacitor, and the gate structure.

[c3] 3.The mixed-mode process of claim 2 wherein the first polysilicon layer is adoped polysilicon layer or an undoped polysilicon layer followed by an ion implantation

process.

[c4] 4.The mixed-mode process of claim 2 wherein a polycide layer is formed before performing the first PEP process, and portions of the polycide layer is removed by the first PEP process.

[c5] 5.Themixed-mode process of claim 4 wherein portions of the first polysilicon layer and the polycide layer in the gate structure is employed as a gate of the MOS transistor of the integration circuits.

[c6] 6.Themixed-mode process of claim 4 wherein portions of the first polysilcion layer and the polycide layer in the bottom electrode plate structure is employed as a bottom electrode plate of the capacitor.

[c7] 7.The mixed-mode process of claim 4 wherein the polycide layer comprises tungsten silicide.

[c8] 8.The mixed-mode process of claim 2 wherein the first type dopants are N-type dopants and the second type dopants are P-type dopants.

[c9] 9.Themixed-mode process of claim 2 wherein the first dopants are P-type dopants and the second type dopants are N-type dopants.

[c10] 10.The mixed-mode process of claim 2 wherein the sec-

ond PEP utilizes the IPO layer as a stop layer.

[c11] 11.The mixed-mode process of claim 2 wherein a wet dip process is performed after the second PEP to remove portions of the IPO layer and to preserve the IPO layer between the bottom electrode plate structure and the top electrode plate employed as a capacitor dielectric layer of the capacitor.

[c12] 12.The mixed-mode process of claim 2 wherein the dielectric layer comprises tetra-ethyloxysilane (TEOS).

[c13] 13.The mixed-mode process of claim 2 wherein either portions of the surface of the semiconductor substrate within the first conductive region, the second conductive region, or the capacitor region comprise a field oxide layer, and surfaces of the field oxide layer and the gate oxide layer are employed as a stop layer for the second etching process used for the formation of the spacers.

[c14] 14.The mixed-mode process of claim 1 wherein the conductors in the first conductive region and the second conductive region are employed as resistors of the integration circuits, and the mask is a high resistance (HR) mask.

[c15] 15.The mixed-mode process of claim 1 wherein the method for controlling the end of the first etching pro-

cess comprises using a time mode or an endpoint mode.

[c16] 16.The mixed-mode process of claim 1 wherein a second ion implantation process is performed to form a source and a drain of the MOS transistor in portions of the semiconductor substrate adjacent to either sides of the gate structure.

[c17] 17.A mixed-mode process for integration circuits comprising:
providing a semiconductor substrate, a surface of the semiconductor substrate comprising at least a first conductor formed in a first conductive region, at least a second conductor formed in a second conductive region, at least a metal-oxide-semiconductor (MOS) transistor formed in a MOS transistor region, and at least a capacitor formed in a capacitor region;
forming a mask on the semiconductor substrate to cover the MOS transistor, the first conductor, and the capacitor and to expose the second conductor;
performing a first ion implantation process to dope the second conductor with first type dopants; and
performing a first etching process to remove a specific thickness of the second conductor.

[c18] 18.The mixed-mode process of claim 17 further comprising the following steps for forming the first conduc-

tor, the second conductor, the MOS transistor, and the capacitor:

sequentially forming a gate oxide layer and a first polysilicon layer on the semiconductor substrate;

performing a first photo-etching-process (PEP) to remove portions of the first polysilicon layer to simultaneously form a gate structure and a bottom electrode plate structure of the capacitor respectively in the MOS transistor region and the capacitor region;

sequentially forming an inter polysilicon oxide (IPO) layer and a second polysilicon layer doped with second type dopants on the semiconductor substrate to cover the gate structure and the bottom electrode plate structure;

performing a second PEP to remove portions of the second polysilicon layer to form the first conductor, the second conductor, and a top electrode plate of the capacitor, respectively, in the first conductive region, the second conductive region, and the capacitor region;

forming a dielectric layer on the semiconductor substrate to cover the first conductor, the second conductor, the gate structure, and the capacitor; and

performing a second etching process to remove portions of the dielectric layer to form a spacer on either sides of the first conductor, the second conductor, the capacitor, and the gate structure.

[c19] 19.The mixed-mode process of claim 18 wherein the first polysilicon layer is adoped polysilicon layer or an undoped polysilicon layer followed by an ion implantation process.

[c20] 20.The mixed-mode process of claim 18 wherein a polycide layer is formed before performing the first PEP process, and portions of the polycide layer is removed by the first PEP process.

[c21] 21.Themixed-mode process of claim 20 wherein portions of the first polysilicon layer and the polycide layer in the gate structure is employed as a gate of the MOS transistor of the integration circuits.

[c22] 22.The mixed-mode process of claim 20 wherein portions of the first polysilcion layer and the polycide layer in the bottom electrode plate structure is employed as a bottom electrode plate of the capacitor.

[c23] 23.The mixed-mode process of claim 20 wherein the polycide layer comprises tungsten silicide.

[c24] 24.The mixed-mode process of claim 18 wherein the first type dopants are N-type dopants and the second type dopants are P-type dopants.

[c25] 25.The mixed-mode process of claim 18 wherein the

first dopants are P-type dopants and the second type dopants are N-type dopants.

[c26] 26.The mixed-mode process of claim 18 wherein the second PEP utilizes the IPO layer as a stop layer.

[c27] 27.The mixed-mode process of claim 18 wherein a wet dip process is performed after the second PEP to remove portions of the IPO layer and to preserve the IPO layer between the bottom electrode plate structure and the top electrode plate employed as a capacitor dielectric layer of the capacitor.

[c28] 28.The mixed-mode process of claim 18 wherein the di-electric layer comprises tetra-ethyloxysilane (TEOS).

[c29] 29.The mixed-mode process of claim 18 wherein either portions of the surface of the semiconductor substrate within the first conductive region, the second conductive region, or the capacitor region comprise a field oxide layer, and surfaces of the field oxide layer and the gate oxide layer are employed as a stop layer for the second etching process used for the formation of the spacers.

[c30] 30.The mixed-mode process of claim 17 wherein the conductors in the first conductive region and the second conductive region are employed as resistors of the inte-gration circuits, and the mask is a high resistance (HR)

mask.

[c31] 31.The mixed-mode process of claim 17 wherein the method for controlling the end of the first etching process comprises using a time mode or an endpoint mode.

[c32] 32.The mixed-mode process of claim 17 wherein a second ion implantation process is performed to form a source and a drain of the MOS transistor in portions of the semiconductor substrate adjacent to either sides of the gate structure.